

Transistor performance of top rough surface of pentacene measured by laminated double insulated-gate supported on a poly(dimethylsiloxanes) base structure

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We report the fabrication and electrical characterization of pentacene field-effect transistors with a laminated double insulated-gate using poly(dimethylsiloxanes) (PDMS) as their supporting structure. The ability of PDMS to conform to surfaces enables us to directly evaluate the device performance of the top rough surface of the pentacene active layer (the pentacene-air interface). The mobility measured for the top surface was only about 20% slightly lower than that of the bottom surface. Device stability under ambient conditions is evaluated. This device structure is useful for the characterization of electrical transport in both the top and bottom surface of a thin film simultaneously. © 2006 American Institute of Physics. [DOI: 10.1063/1.2166488]

Organic thin-film field-effect transistors (OTFTs) have shown promising potential for applications not only in large-area electronics, such as electronic papers¹⁻³ and flat panel displays,⁴ but also for sensors,^{5,6} smart cards, and radio-frequency identification tags (RFIDs).^{7,8} The motivation comes mainly from the ease of fabrication (low-temperature deposition and solution processing) and mechanical flexibility of organic materials. In particular, pentacene OTFTs have shown very good device performance with mobilities greater than $1 \text{ cm}^2/\text{V s}$.⁹⁻¹¹ While these devices were fabricated with pentacene evaporated directly onto the dielectric surface, it is sometimes desirable to deposit the dielectric layer on the top surface of pentacene. There have been few reports of such devices, with the best reported mobility about $0.02 \text{ cm}^2/\text{V s}$,^{12,13} which is much lower than the best reported values for pentacene. While it is known that exposure to humidity^{5,14-19} and photo-oxidation¹⁸⁻²¹ can lead to pentacene device degradation, it is unclear whether the mobility of the top surface is intrinsically much lower than that of the bottom surface. Furthermore, it is unknown whether the lower mobility is mainly caused by high surface roughness, lack of good molecular ordering on the surface of a thick film, chemical degradation from the dielectric layer deposition process, or exposure to air and moisture which could lead to trapping by oxygen and moisture at the dielectric/pentacene interface. In this work, we use laminated double insulated-gate thin-film transistor (TFTs) having poly(dimethylsiloxanes) (PDMS) as the dielectric layer as well as the substrate to measure both the top and bottom surfaces on the same pentacene film.²² The PDMS stamp allows us to make conformal contact with pentacene without using deposition methods for dielectric layer that may cause degradation to the pentacene surface.²²

Figure 1 inset shows the schematic structure of a pentacene field-effect transistor with a laminated, double insulated-gate structure. Highly doped n^{++} silicon wafers

with thermally grown 300 nm silicon dioxide (capacitance $C_i=10 \text{ nF/cm}^2$) were cleaned by rising with acetone followed by isopropyl alcohol. A pentacene layer (60 nm) was subsequently deposited at a pressure less than 2×10^{-6} Torr with a deposition rate of 0.5 \AA/s . Tapping mode AFM (Digital Instruments) data showed that the average peak-to-valley roughness of the top surface of the polycrystalline pentacene film is about 49.6 nm, with a root-mean-square (rms) roughness of about 7.5 nm, much rougher than the surface of SiO_2 with a peak-to-valley roughness of 2 nm and rms roughness of 0.2 nm.¹⁰

A piece of PDMS was used to prepare the top-gate device using similar procedures as previously reported.²² The dielectric layer was a PDMS layer with a capacitance of 2.9 nF/cm^2 . The channel width and channel length are $2000 \mu\text{m}$ and $100 \mu\text{m}$, respectively. To complete the fabrication of the double insulated-gate TFT, the above PDMS structure was laminated on top of a piece of Si/ SiO_2 wafer with a pentacene film to give the device structure, shown in the inset of Fig. 1. Prior to lamination inside a glove box

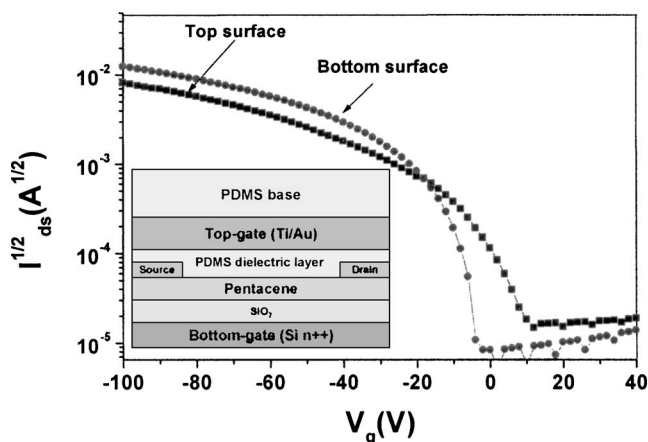


FIG. 1. I - V characteristics of (a) top surface and (b) bottom surface devices. Inset: Schematic structure for a double insulated-gate pentacene field-effect transistor.

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($H_2O < 0.1$ ppm, $O_2 \sim 1$ ppm), the PDMS structure was placed inside the glove box for more than 12 h to minimize the moisture and oxygen absorbed on the surface of PDMS. Electrical characterization was carried out using a Keithley 4200SCS semiconductor parameter analyzer, during which the unused gate is always grounded. Figure 1 shows the typical current-voltage (I - V) characteristics for top and bottom surface devices.

The calculated mobilities at the saturation region of the top surface were typically between $0.1 \text{ cm}^2/\text{V s}$ and $0.2 \text{ cm}^2/\text{V s}$ for devices measured immediately after lamination, which is 11% to 37% lower than those of the corresponding bottom surface device regardless of whether the initial lamination was carried out inside or outside the glove box. The high mobility of the top surface is an indication of a high degree molecular ordering of pentacene molecules in the top surface layer even in a thick film. This is consistent with our observation that pentacene molecules retain a high degree of crystallinity and molecular orientation throughout the film up to 100 nm in thickness, observed with 2D grazing incidence x-ray diffraction.²³ The slightly lower mobility of the top surface for the laminated devices may be related to a high surface roughness, slight change in molecular orientation, grain size, and poor contact between pentacene and the dielectric layer. But surprisingly, the roughness did not significantly decrease the mobility. This result indicates that it is possible to make high-performance devices using the top surface of pentacene.

For devices laminated outside of the glovebox and then stored in the lab environment, the mobility and on/off ratio [the ratio of I_{ds} at $V_g = -100$ (V) in the saturation regime divided by the minimum value of I_{ds} , typically at $V_g \geq 0$ (V)] were reduced by more than 50% and 60%, respectively, due to exposure to air and light for about a week (see Figs. 2(a) and 2(b)). They were reduced by a lesser extent ($\sim 30\%$, 50%, respectively) after being exposed only to air but without exposure to ambient light for the same amount of time. All TFTs stored under an ambient lab environment had almost completely degraded after a few weeks. For devices laminated inside of the glovebox and then stored in the lab environment, a similar trend was observed. The on/off current ratio decreases as a function of time for all devices regardless of whether they were exposed to light. We believe the on-current decreases as a function of time as a result of the chemical degradation of pentacene, and the off-current increases as a function of time due to p doping by oxygen.^{24,25}

As a reference, the effect of air and light on the performance of the corresponding smooth bottom surface was also monitored. A slower device degradation than the top surface was observed. After being stored in air with exposure to ambient light for ten days, the bottom surface mobility is at least one order of magnitude higher than its corresponding top-surface device, suggesting that pentacene degradation starts on the top surface and slowly extends to the bottom surface. After twenty days, the mobilities for the bottom and top surface became similar ($0.02 \text{ cm}^2/\text{V s}$ and $0.01 \text{ cm}^2/\text{V s}$, respectively) indicating that the degradation of the pentacene film has extended to the bottom surface. I_{ds} versus V_g for the top and bottom surfaces of pentacene was plotted in Figs. 3(a) and 3(b), respectively.

For comparison, we also used vapor deposited parylene (2300 nm, dielectric constant $\epsilon = 2.6$) as a dielectric layer on

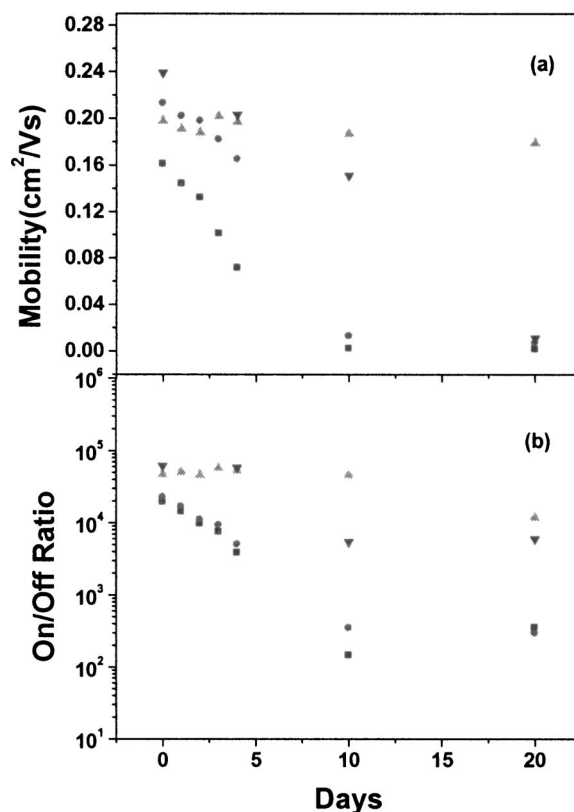


FIG. 2. (a) Charge carrier mobility and (b) on/off ratio associated with the rough top surface of pentacene as a function of time for devices laminated outside the glovebox. ■: Exposed to air and ambient light; ●: Exposed to air only; ▲: Stored inside the glovebox; and ▼: Mobility and on/off ratio associated with the bottom smooth surface of pentacene with exposure to air and ambient light.

pentacene. Parylene is known to form a good conformal contact and has been used as a dielectric layer for organic single-crystal transistors.²⁶ The top surface mobility was about $0.09 \text{ cm}^2/\text{V s}$ while the bottom surface mobility was $0.55 \text{ cm}^2/\text{V s}$. The pentacene active layer in this experiment had been exposed to ambient conditions for five days before parylene deposition. The mobility is similar to that measured using the PDMS double insulated-gate device as described earlier with pentacene films deposited at the same time and after the same amount of exposure to air.

We also used a PDMS layer (about $1 \mu\text{m}$) directly spin-coated onto the top surface of pentacene as a dielectric layer followed by deposition of the gate electrode. The top surface mobility was $0.15 \text{ cm}^2/\text{V s}$ measured immediately for a fresh device, which is in the same range as the corresponding laminated device described above. The mobility for this type of device with exposure to air and light was reduced by 30% after one week, 45% after two weeks, and then 76% by Day 20. The degradation rate is slower than the corresponding device made by lamination. This may be a result of a better conformal contact with spincoated PDMS than by lamination, which may slow down the diffusion of oxygen and moisture.

It is known that pentacene is easily photo-oxidized resulting in device performance degradation.²⁷ In order to further understand the degradation of pentacene, top-contact pentacene TFTs were exposed to an ultraviolet (UV) light source ($\lambda = 254 \text{ nm}$) in air. The mobility initially slowly decreased from 0.32 to $0.25 \text{ cm}^2/\text{V s}$ (Fig. 3 inset). After 10 h,

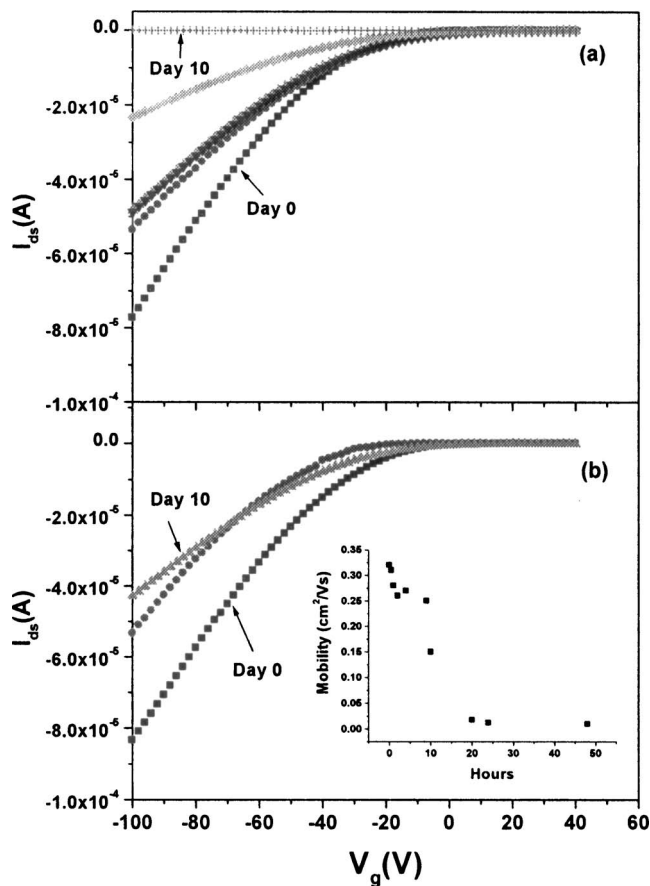


FIG. 3. (a) I_{ds} vs V_g for the top surface of pentacene devices laminated outside glovebox. ■: Day 0; ●: Day 1; ▲: Day 2; ▼: Day 3; ◆: Day 4; and +: Day 10. (b) I_{ds} vs V_g for the bottom surface of pentacene devices laminated outside the glove box. ■: Day 0; ●: Day 4, and ▲: Day 10. Inset: Mobility as a function of time for pentacene devices exposed to 254 nm UV light.

the mobility began to decrease sharply. This is because that photo-oxidation starts from the top surface of pentacene. Before degradation reaches the interface between pentacene and the dielectric layer, where the majority amount of the current flow takes place, no significant decrease in mobility is observed. Moisture does not cause chemical degradation to pentacene. However, it can be trapped in the grain boundaries and at the interface between the pentacene and dielectric layer causing a decrease in mobility.^{15,28–30}

In summary, we have prepared and characterized pentacene transistors using laminated double insulated-gate structure. The charge carrier mobility and on/off current ratio for the top rough surface of the pentacene active layer has been successfully measured. It was found that the top surface has only slightly lower mobility than the bottom surface, despite its high degree of roughness. The degradation of device performance for the rough top surface of pentacene in air is faster than the smooth bottom surface of pentacene. This study allows us to gain better insight into the limitations of organic transistors with different device configurations. The lamination approach is a convenient method to prepare top-gate structures. Finally, this device structure also allows characterization of both the top and bottom surface of the same film, which provides important information of whether long-range order is retained throughout the film.

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