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Temperature gradient controlled crystal growth from TIPS pentacene-poly(α-methyl styrene) blends for improving performance of organic thin film transistors

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ABSTRACT

6,13-bis(triisopropylsilylethynyl) pentacene (TIPS pentacene) from simple drop casting typically forms crystals with random orientation and poor areal coverage, which leads to device-to-device performance variation of organic thin film transistors (OTFTs). Previously, a temperature gradient technique was developed to address these problems. However, this approach simultaneously introduced thermal cracks due to the thermally induced stress during crystallization. These thermal cracks accounted for a reduction of charge transport, thereby impacting the device performance of TIPS pentacene based OTFTs. In this work, an insulating polymer, poly(α-methyl styrene) (PαMS) was blended with TIPS pentacene to relieve the thermal stress and effectively prevent the generation of thermal cracks. The results demonstrate that the incorporation of PαMS polymer combined with the temperature gradient technique improves both the hole mobility and performance consistency of TIPS pentacene based OTFTs.
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1. Introduction

The performance of organic thin-film transistors (OTFTs) based on solution-grown organic small-molecule semiconductors, such as 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS pentacene) [1–3], 5,11-bis(triethylsilylethynyl) anthradithiophene (TES-ADT) [4–6], and 2,7-dioctyl [1]benzothieno[3,2-b] [1] benzothiophene (C_8-BTBT) [7–9], has notably advanced in recent years. The enhancement in OTFT performance situates these small-molecule semiconductors at the forefront as promising candidates for the next-generation large-area flexible electronics [10–12]. Nevertheless, maintaining device-to-device performance uniformity of these small-molecule based OTFTs still remains a challenge [13,14] because of the non-uniform crystal orientation in the active layer [15,16]. Recently, we developed a simple yet unique solution processing method, the temperature gradient technique, to control crystal growth of pure TIPS pentacene semiconductor [17]. With such an approach, the intrinsic crystal misalignment is reduced, and the resulting film exhibits large crystal sizes and substantial areal coverage. The temperature gradient technique, however, simultaneously introduces thermal cracks, which impact charge transport and reduce the hole mobility of TIPS pentacene OTFTs [18,19]. Therefore, it is mandatory to eliminate the thermal cracks in the TIPS pentacene films in order to realize high-performance OTFTs.

The long chains of polymers are anticipated to provide a flexible matrix to the TIPS pentacene crystals which could relieve the thermal stress, thereby preventing the occurrence of thermal cracks associated with the temperature gradient technique. In addition, various polymer additives, particularly poly(α-methyl styrene) (PαMS) [20], have demonstrated a vertical phase segregation within the TIPS pentacene active layer, improving charge transport [21,22]. Therefore, it is expected that incorporating PαMS into TIPS pentacene could result in an enhancement of OTFT performance by preventing thermal cracks and utilizing its capability to increase charge transport of TIPS pentacene film [23,24].

In this study, we demonstrate that incorporation of the insulating polymer, PαMS, into TIPS pentacene is able to effectively prevent the generation of thermal cracks and further enhance crystal alignment in the temperature gradient approach. As a result, the average mobility and device performance consistency have been improved. This crystal growth method which applies temperature gradient to a TIPS pentacene/PαMS blend is also employed to fabricate TIPS pentacene OTFTs on ITO/polyethylene terephthalate (PET) flexible substrate with poly(4-vinylphenol) (PVP)

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as the gate dielectric. Maximum hole mobilities of 0.25 cm^2/V and 0.5 cm^2/V were achieved from TIPS pentacene/PαMS OTFTs on SiO_2/Si and ITO/PET flexible substrates, respectively.

2. Experiment

TIPS pentacene, PVP (molecular weight $M_w = 25$ k) and toluene (anhydrous, 99.8%) were purchased from Sigma Aldrich. PαMS ($M_w = 108$ k) with a polydispersity index of 1.02 was purchased from Polymer Standards Service. All materials were used as received without further purification. A temperature gradient was established by heating one side of a petri dish while the other side was kept in ambient air for 30 min in order to reach thermal stability. A heavily doped *n*-type silicon substrate with a 300 nm thickness of SiO_2 layer was positioned on the petri dish in the established temperature gradient region for an additional 15 min to reach the desired temperature. The temperatures were measured using a type-K thermocouple beaded probe.

To form an active layer, TIPS pentacene/PαMS blends in toluene (5 mg/mL) were drop casted onto the substrate inside the petri dish. The samples were then sealed inside the petri dish with a few layers of parafilm, allowing crystallization in a solvent rich environment. The slow solvent evaporation facilitates crystal growth, leading to large crystal sizes. The temperature gradient employed for crystal growth was around 3 °C/cm–5.5 °C/cm. Optical micrographs of TIPS pentacene/PαMS blend films were taken using a Zeiss Axioplan optical microscope with a built-in camera, and the film topography was characterized using Vecco Dektak Series V profilometer. After the formation of the TIPS pentacene active layer, 50 nm gold (Au) was deposited through a shadow mask via thermal evaporation as the OTFT source and drain contacts. In addition, TIPS pentacene/PαMS OTFTs were also fabricated on flexible ITO/PET substrates with a PVP polymer layer as gate dielectric. To form the gate dielectric layer, PVP and a cross-linking agent, poly(melamine-*co*-formaldehyde) methylated solution (PMF), were first mixed (1:1 wt ratio) in propylene glycol monomethyl ether acetate (PGMEA ≥ 99.5%) at a concentration of 8 wt%, and stirred for 24 h. After the PVP-PMF in PGMEA solution was spin coated onto clean ITO/PET substrates at 2000 rpm for 60 s, the substrates were cured at 180 °C in a vacuum oven for 30 min to generate thermal cross-linking in the PVP layer. The thickness of the PVP-PMF dielectric layer was measured to be 280 nm with cross-sectional SEM imaging (JOEL 7000 Scanning Electron Microscope). As the final step, Au was deposited on the ITO/PET flexible substrates to complete the OTFT fabrication. The thickness of the source and drain electrodes was 100 nm to accommodate the active layer's large surface roughness.

Electrical characterization of OTFTs was performed in an ambient environment at room temperature using an Agilent B1500A semiconductor parameter analyzer. Field-effect hole mobility in the saturation regime was extracted from the slope of the transfer characteristic $(I_{DS})^{1/2}$-V_{GS}, based on the traditional MOSFET equation:

$$I_{DS} = \mu C_i \frac{W}{2L}(V_{GS} - V_T)^2 \quad (1)$$

where μ is the saturation mobility, C_i is the capacitance of the gate dielectric per unit area, W and L are the OTFT channel width and length, respectively, and V_T is the threshold voltage.

All devices were measured three times to ensure the consistency of the extracted mobilities. The capacitance of the 300 nm silicon dioxide is 11.50 nF/cm^2. The capacitance of PVP dielectric layer was extracted from capacitance-voltage measurement to be 10.75 nF/cm^2.

3. Results and discussion

Fig. 1 illustrates how the temperature gradient method works to effectively align the TIPS pentacene crystals. The temperature gradient leads to a solubility difference within the solution, which results in a higher density of nucleation seeds in the lower temperature region. The TIPS pentacene crystal growth commences from the lower temperature region towards the higher temperature region when the solution reaches supersaturation, as shown in Fig. 1(a–c). With the incorporation of PαMS polymer, thermal cracking that could have developed in the crystalline film is eliminated and the uniformity of crystal orientation is further improved. The well-aligned crystals, enhanced areal coverage, and film uniformity are achieved by the combination of the temperature gradient technique and the addition of the PαMS polymer, which is illustrated in the cartoon of Fig. 1(d) and also demonstrated over the entire substrate in the digital image of Fig. 1(e).

Fig. 2(a–c) show the morphologies of pure TIPS pentacene films with the application of the temperature gradient technique. Employing a temperature gradient overcomes the random orientation of crystals and poor areal coverage as compared to those films from simple drop casting [12,17]; however, the temperature gradient method also causes the development of undesired thermal cracks in the film as observed in these images. Fig. 2(d–f) show the morphologies of the TIPS pentacene films with the addition of PαMS polymer, in which no thermal cracks are generated. As noticed, the crystal width is smaller when compared to those without the addition of PαMS polymer. It is anticipated that the reduced crystal width, along with PαMS polymer matrix within the film, effectively relieves the thermally induced stress and thereby prevents the generation of thermal cracks during crystallization. Among the TIPS pentacene/PαMS films, three different TIPS pentacene to PαMS blending ratios, 1:1, 2:1 and 3:1, were examined, but no major differences in morphology in terms of crystal size, areal coverage and crystal orientation were observed. It is worth mentioning that the stripes between the well-oriented TIPS pentacene crystals in these images result from TIPS pentacene/PαMS molecules that were not fully crystallized but deposited onto the substrate. The stripe regions of the film are more amorphous rather than crystalline. The film topography shown in Fig. 3 demonstrates a more uniform surface profile of the TIPS pentacene/PαMS film compared with that of pure TIPS pentacene from simple drop casting; thereby indicating an improvement in the surface smoothness and uniformity from the polymer/small-molecule blend with the temperature gradient method.

Bottom-gate, top-contact OTFTs were fabricated to test charge transport in the TIPS pentacene/PαMS blend film. Fig. 4(a) and (b) show the transfer and output curves of the TIPS pentacene/PαMS based OTFTs obtained from the optimal blend ratio of 2:1 at a 3.5 °C/cm temperature gradient, respectively. The slight nonlinearity in the subthreshold region of the output curves indicate large contact resistance of drop cast TIPS pentacene OTFTs with a top contact, bottom gate structure [25,26]. A threshold voltage V_T around 5 V, current on/off ratio greater than 5×10^4, and subthreshold swing of 2.6 V/dec were extracted from the transfer characteristics.

To demonstrate the potential of the solution processed TIPS pentacene/PαMS film via the temperature gradient approach for flexible device applications, OTFTs were also fabricated on flexible ITO/PET substrates. Cross-linked PVP-PMF was used as the gate dielectric because it is chemically inert against the toluene solvent used to dissolve the TIPS pentacene/PαMS blends, and PVP has a well matched surface energy with TIPS pentacene [27], thereby promoting the adhesion of the hydrophobic silyl groups of TIPS pentacene to the substrate. Fig. 5(a) shows the device configuration

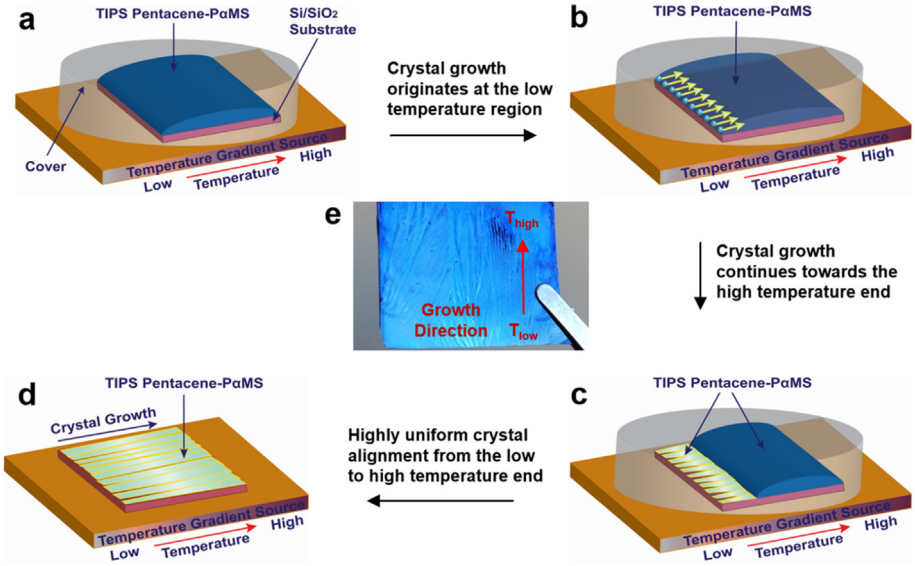

Fig. 1. (a–d) Schematic of crystal growth using the temperature gradient technique. (e) A digital image of the resultant TIPS pentacene crystals from the combination of the temperature gradient technique and addition of PαMS polymer.

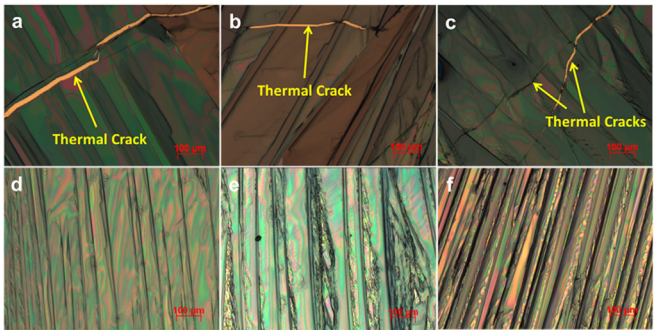

Fig. 2. Polarized optical micrographs of (a–c) pure TIPS pentacene films showing large crystals with thermal cracks and (d–f) TIPS pentacene/PαMS blend films showing relatively small crystals without any cracks.

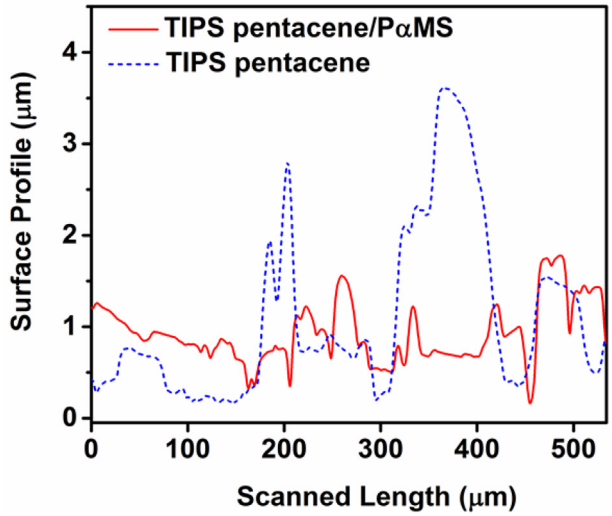

Fig. 3. Comparison of film topography between TIPS pentacene/PαMS film via the temperature gradient technique and pure TIPS pentacene from simple drop casting.

of bottom-gate, top-contact TIPS pentacene/PαMS OTFTs with PVP-PMF dielectric on the ITO/PET substrate. The corresponding digital image of patterned OTFTs is presented in Fig. 5(b). Fig. 5(c) and (d) show the transfer and output characteristics acquired from the best TIPS pentacene/PαMS OTFTs on ITO/PET substrates, respectively. A threshold voltage V_T around −4 V, current on/off ratio greater than 10^3, and subthreshold swing of 3.3 V/dec were obtained.

In order to extract the mobility, parallel plate capacitors (ITO–(PVP-PMF) –Au) were fabricated and capacitance-voltage measurements were performed to determine the capacitance. The capacitance per unit area measured in accumulation regime with a bias voltage of −20 V was attained as 10.75 nF/cm^2. The average mobility along with the standard deviation of mobility was calculated to be 0.37 ± 0.12 cm^2/V from the measurement of five OTFTs. The highest field-effect hole mobility was extracted to be 0.5 cm^2/V. For comparison, a maximum average mobility of 0.18 ± 0.07 cm^2/V and the highest hole mobility of 0.25 cm^2/V were obtained from TIPS pentacene/PαMS OTFTs on silicon substrate. The higher mobility on ITO/PET flexible substrate is attributed to the hydrophobic nature of PVP-PMF dielectric surface, which promotes the adhesion of silyl group from TIPS pentacene and molecular stacking [28]. Compared with an average mobility of 0.06 ± 0.05 cm^2/V from pure TIPS pentacene via temperature gradient method only, the mobility increased from the order of magnitude of 10^{-2} cm^2/V [17] to about 10^{-1} cm^2/V for the TIPS pentacene/PαMS blend based OTFTs in this work. The increase in mobility is mainly attributed to the improvement of crystal orientation and elimination of the thermal cracks. The average mobilities are summarized in Fig. 6(a). It is worth mentioning that, although hexamethyldisilazane (HMDS) treatment has been employed in most literature works to passivate the silanol groups on the silicon dioxide surface to enhance charge transport [25], this treatment was not utilized in this study since the TIPS pentacene/PαMS solution suffered from severe dewetting on the HMDS treated surface, which considerably reduced the film areal coverage.

In addition, the performance consistency, which is defined as the ratio of the average mobility (μ_{Avg}) to the standard deviation of mobility (μ_{Stdev}), was also calculated. As shown in Fig. 6(b), the pure TIPS pentacene based OTFTs exhibit μ_{Avg}/μ_{Stdev} of 1.2, whereas TIPS pentacene/PαMS OTFTs on silicon substrate and ITO/PET flexible

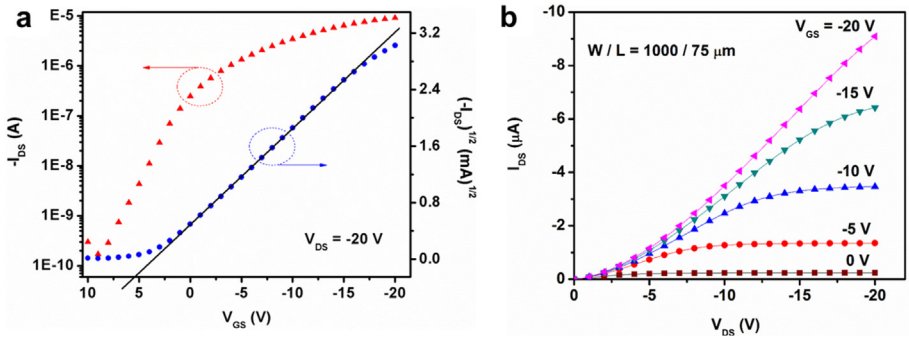

Fig. 4. (a) Transfer and (b) output characteristics of bottom-gate, top-contact TIPS pentacene/PαMS OTFTs from the optimal blend ratio of 2:1 at a 3.5 °C/cm.

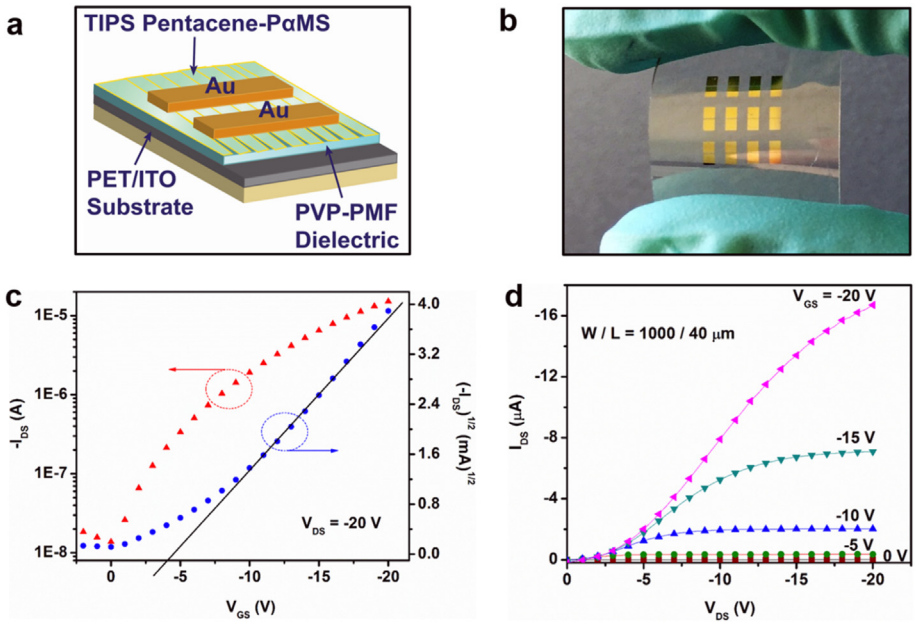

Fig. 5. (a) Device configuration of bottom-gate, top-contact TIPS pentacene/PαMS OTFTs. (b) A digital picture that shows the OTFTs on ITO/PET flexible substrate. (c) Transfer and (d) output characteristics of TIPS pentacene/PαMS OTFTs on ITO/PET flexible substrate.

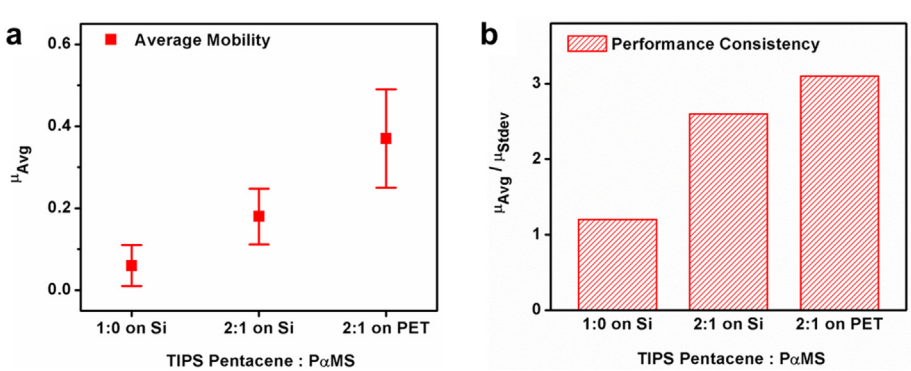

Fig. 6. (a) Average hole mobility and (b) corresponding performance consistency of pure TIPS pentacene based OTFTs (1:0 blend ratio), and TIPS pentacene/PαMS based OTFTs (2:1 blend ratio) on silicon and ITO/PET substrates, respectively.

substrate show μ_{Avg}/μ_{Stdev} of 2.6 and 3.1, respectively, indicating effective improvement of OTFT performance consistency.

4. Conclusions

In summary, we demonstrated that employing a temperature gradient technique coupled with the addition of a PαMS insulating polymer not only significantly improves the crystal alignment and

enhances areal coverage of the TIPS pentacene film, but also concurrently eliminates the thermal cracks introduced by the application of a temperature gradient. The elimination of thermal cracks promotes charge transport and increases mobility from the order of magnitude of 10^{-2} cm^2/V via the temperature gradient technique only to about 10^{-1} cm^2/V, in this work. The effectiveness and versatility of the temperature gradient method with the incorporation of PαMS polymer was also demonstrated on a flexible ITO/PET substrate, and a hole mobility of 0.5 cm^2/V was obtained.

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